

## CHAPTER 5

### THE LOGIC INTERFACE

#### 5.1 LEVEL SHIFTERS

Most CMOS DACs include a TTL to CMOS level shifter at each digital input to translate the external TTL input logic levels to the internal CMOS logic levels used in the DAC. There are two basic types of level shifter. One gives TTL compatibility only when the supply voltage  $V_{DD}$  is +5V—for other values of  $V_{DD}$  it is CMOS compatible but not TTL compatible. A second type gives CMOS and TTL compatibility for all permissible supply voltages. Appendix 1 summarizes these features for Analog Devices' DACs.

The supply current ( $I_{DD}$ ) drawn by a DAC is chiefly determined by the input logic levels. Figure 5.1 shows the variation in  $I_{DD}$  as a single digital input is swept from 0V to +5V. The voltage at which the current peak occurs varies from DAC to DAC but it is clear that to minimize  $I_{DD}$  the input logic levels

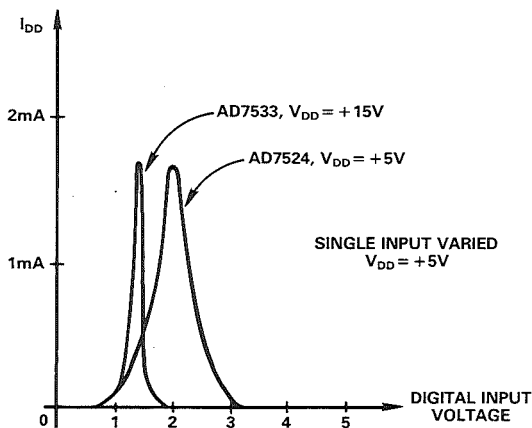


Figure 5.1 Typical  $I_{DD}$  vs. Digital Input Voltage

should be as close to the 0 and +5 volt supply rails as is practical. Pull-up resistors at the digital inputs can often help to reduce DAC power consumption.

#### 5.2 MICROPROCESSOR COMPATIBLE DACs

A "Microprocessor Compatible DAC" includes one or more sets of registers to hold the digital value to be applied to the DAC. The simplest microprocessor compatible DACs incorporate a single register which is loaded in parallel from the data bus under the control of the  $\overline{CS}$  (chip select) and  $\overline{WR}$  (write) pins. This scheme is used for the AD7524, AD7528 and AD7545 shown in Figures 5.2, 5.3 and 5.4 respectively. When  $\overline{CS}$  and  $\overline{WR}$  are both low, the DAC register is transparent and information on the data bus passes directly to the DAC inputs. *If the data bus changes during this time, the inputs to the DAC will change and "noise glitches" may appear on the output.* The data from the bus is latched when  $\overline{CS}$  or  $\overline{WR}$  goes high. The AD7528 contains two DACs and only

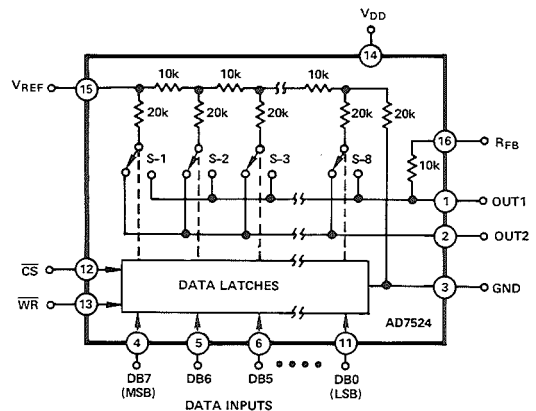


Figure 5.2 AD7524 8-Bit DAC - 16-Pin DIP

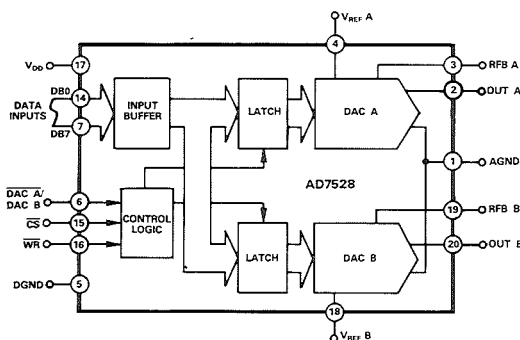


Figure 5.3 AD7528 – Dual 8-Bit DAC – 20-Pin DIP

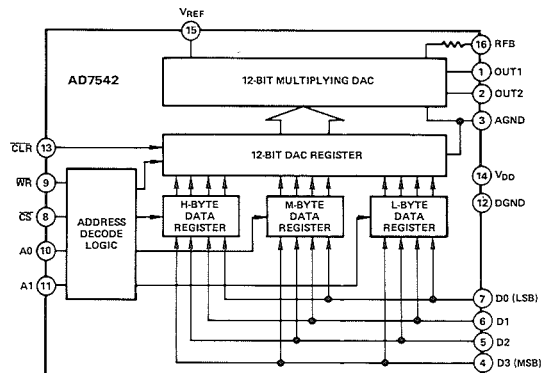


Figure 5.5 AD7542 12-Bit DAC – 16-Pin DIP

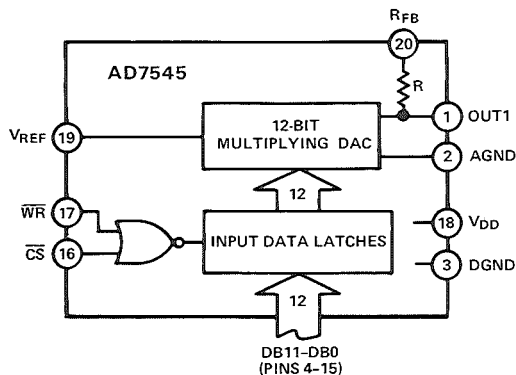


Figure 5.4 AD7545 12-Bit DAC – 20-Pin DIP

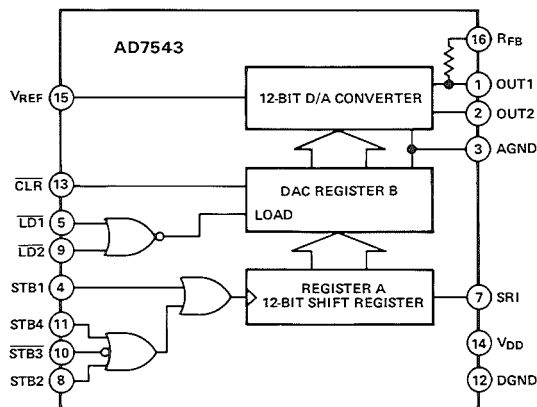


Figure 5.6 AD7543 12-Bit DAC – 16-Pin DIP

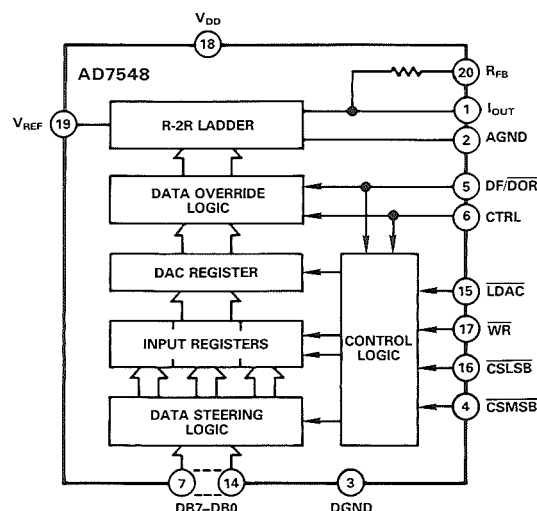


Figure 5.7 AD7548 12-Bit DAC – 20-Pin DIP

the latches associated with the addressed latch are transparent when  $\overline{CS}$  and  $\overline{WR}$  are low.

In many applications the system bus width is insufficient to load the full data word to the DAC in a single byte; and the data word is therefore transmitted to the DAC in two or more bytes. Additional registers are used on-chip to reassemble the bytes into the full parallel word before it is presented to the DAC. The AD7542, AD7543 and AD7548 shown in Figures 5.5 through 5.7 all incorporate a two register arrangement known as double buffering. The AD7548 (12-bits) is designed to be loaded in 8-bit bytes and is therefore suitable for most 8-bit bus systems including those of the 8088 and 68008 16-bit microprocessors. The AD7542 is loaded by three 4-bit nibbles and can connect directly to the 4-bit expansion port of MCS48 series of microprocessors. The AD7543 is loaded serially. Since multiple byte input to a DAC requires fewer digital input pins than a full parallel input the “free” pins on the dual-in-line package are used to provide features such as additional chip select pins, internal register reset, etc. The list below sum-

marizes various logic features available in the AD7XXX line of microprocessor compatible DACs.

**DAC register reset** (AD7542, AD7543) sets the contents of the register equal to zero. This is useful in power-up situations requiring the DAC have zero output at switch-on.

**Additional chip select pins** having a chip-select function found on the AD7542 and AD7543 simplify address decoding.

**Pin selectable input format** is available on the AD7548. Data to the DAC may be either left-hand justified (8+4) or right-hand justified (4+8). Pin straps are used to appropriately steer the input bytes to the DAC register.

**Data override** (AD7548) is used to force the digital input word to the DAC to a given code regardless of the contents of the DAC registers. The AD7548 can be forced to zero and full scale. This feature is useful for power-up situations, but more importantly for assisting system calibration because the DAC outputs can be set to known states without having to rely on the host processor to deliver the appropriate codes via special calibration routines.

## 5.3 PRACTICAL INTERFACE DESIGN

### 5.3.1 Data and Address Bus Connections

A TTL logic transition can couple a 30mV noise spike from a single pin across an empty integrated circuit package. It is, therefore, important to design digital-to-analog interface circuits which minimize the amount of noise injected from the high speed digital system into the precision analog circuits. It is good practice to disable all logic signals to the DAC when it is not being addressed. Figure 5.8 shows the general principles involved. The data bus,  $\overline{CS}$  and  $\overline{WR}$  are held to "1" until the DAC address appears on the address bus. The data inputs are then enabled and  $\overline{CS}$  and  $\overline{WR}$  go low at the appropriate time to strobe the data into the DAC. The introduction of the additional gates between the DAC and the microprocessor changes the relative timing of the microprocessor signals and any practical design must take account of this. Programmable logic arrays such as PAL 16L8A are a useful way to reduce the delays and the number of I.C. packages required to buffer the data bus.

Three state buffers should not be used without pull-up resistors in place of the data bus gates. This is because a high impedance indeterminate state at the buffer outputs will significantly increase the power

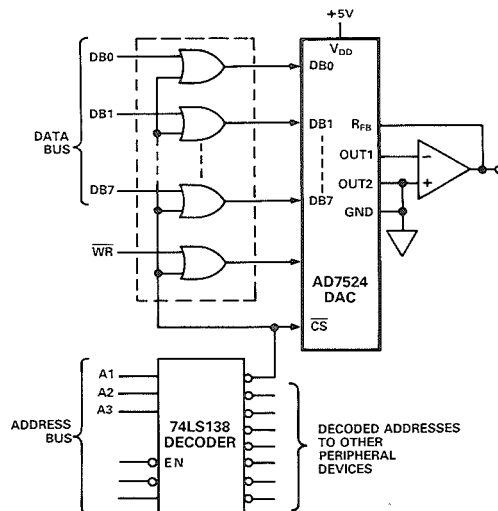


Figure 5.8 General Method of Interfacing DACs to  $\mu P$  Buses

supply current to the DAC (see Section 5.1), and may cause malfunction. The  $\overline{CS}$  and  $\overline{WR}$  signals should only go low when the DAC is addressed—if possible, do not directly connect the microprocessor write signal to the  $\overline{WR}$  pin of the DAC because this signal is continuously active and will therefore create noise at the output of the DAC. Section 6.9 gives some practical circuits for connecting CMOS DACs to microprocessors.

### 5.3.2 Power Supply, Ground Connections and Circuit Board Layout

CMOS DACs have several important features which directly affect the design of power supply connections, circuit board layout, and other interconnection paths. These include:

- OUT1 and OUT2 must be at the same potential. For this reason signal paths from OUT1 and OUT2 to the op amp should not be used to carry other currents (for example ground currents in the OUT2 line).
- Noise on AGND produces noise at the DAC output (see Section 2.2) consequently AGND should be a "quiet" connection.
- Power supply noise produces noise at the DAC output (see Section 2.3.3 on power supply rejection). DAC power supplies should be decoupled and have a separate connection to the power supply line. DACs operating with  $V_{DD} = +5V$  should preferably have a completely separate +5V regulator.

- d) If separate DGND and AGND connections are used, caution must be exercised to prevent excessive voltage differences between the two from occurring during power-up or when plugging-in or removing boards. Normally a pair of IN914 diodes connected in inverse parallel between DGND and AGND can be used to prevent this from happening.

Figure 5.9 shows a typical circuit board layout for the AD7545 12-bit D/A converter with an AD542 output amplifier. The board layout has been spread out a little to show both sides of the board more clearly. Dotted lines are for the underside of the board and full lines for the component side. The connection from the positive input of the op amp (pin 3) is routed first to the AGND (and OUT2) of the DAC (pin 2) and then to the AGND bus line. AGND is also used to form an unclosed guard ring around the OUT1 to the op amp negative input. This guard ring prevents unwanted leakage currents from reaching the OUT1 connection. By leaving the ring incomplete the OUT2 to op amp connection is unaffected. All the ground and supply lines run parallel to one another as shown and should be as broad as is practically possible. In addition to the heavy DGND line, a second finer DGND line threads between pins 18 and 19 as shown to screen the analog section from the digital section of the circuit.

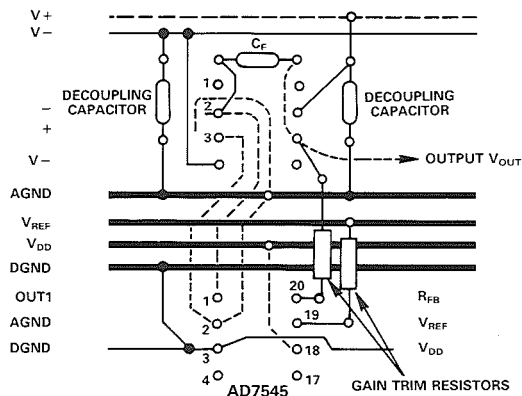


Figure 5.9 Typical Circuit Board Layout for CMOS DAC (AD7545) and Output of Op Amp – Component Side

This screen ties down any stray capacitances and helps minimize digital-analog feedthrough and glitches.

Some solder fluxes and cleaning materials can form slightly conductive films which cause leakage between analog input and output. The user is cautioned to ensure that the manufacturing process for circuits using D/A converters does not allow such a film to form.